CLAIMS

What is claimed is:

1. A method of automatic delay detection and receiver adjustment for a synchronous communications bus system with multiple cycle delays, the method comprising the steps of:

(a) defining a delay detection and calibration phase;

(b) sending a predefined bus signal test pattern for each bus line during the delay detection and calibration phase;

(c) using the predefined bus signal test pattern to determine a longest delay time for each bus line during the delay detection and calibration phase;

(d) adjusting a receiver for each bit line to receive incoming signals at a time based on the determination of step (c); and

(e) placing the bus system in a normal communication mode.

2. In a synchronous communications bus system having a sender subsystem and a receiver subsystem, apparatus for detecting delay and adjusting all receivers in the receiving subsystem, the apparatus comprising:

worst case delay detection circuitry for each bit of the bus system; and

control circuitry coupled to the worst case delay detection circuitry for each bit; operative to select one of two receiver paths for each bit as a function of each bit's delay detection circuitry output and clock signals associated with each bit's receiver latch.

3. The apparatus of Claim 2 wherein at least two of the bits have worst case delay detection circuitry adapted to use different clock phases of the synchronous bus system.